

MULTI-VT SENSING METHOD BY VARYING BIT LINE VOLTAGE

CLAIM OF PRIORITY

[0001] The present application claims priority to U.S. Provisional Application No. 62/172,182, entitled "Multi-VT Sensing Method," filed Jun. 7, 2015, which is herein incorporated by reference in its entirety.

BACKGROUND

[0002] Semiconductor memory is widely used in various electronic devices such as cellular telephones, digital cameras, personal digital assistants, medical electronics, mobile computing devices, and non-mobile computing devices. Semiconductor memory may comprise non-volatile memory or volatile memory. A non-volatile memory allows information to be stored and retained even when the non-volatile memory is not connected to a source of power (e.g., a battery). Examples of non-volatile memory include flash memory (e.g., NAND-type and NOR-type flash memory) and Electrically Erasable Programmable Read-Only Memory (EEPROM).

[0003] Both flash memory and EEPROM utilize floating-gate transistors. For each floating-gate transistor, a floating gate is positioned above and insulated from a channel region of the floating-gate transistor. The channel region is positioned between source and drain regions of the floating-gate transistor. A control gate is positioned above and insulated from the floating gate. The threshold voltage of the floating-gate transistor may be controlled by setting the amount of charge stored on the floating gate. The amount of charge on the floating gate is typically controlled using Fowler-Nordheim (F-N) tunneling or hot-electron injection. The ability to adjust the threshold voltage allows a floating-gate transistor to act as a non-volatile storage element or memory cell. In some cases, more than one data bit per memory cell (i.e., a multi-level or multi-state memory cell) may be provided by programming and reading multiple threshold voltages or threshold voltage ranges.

[0004] NAND flash memory structures typically arrange multiple floating-gate transistors in series with and between two select gates. The floating-gate transistors in series and the select gates may be referred to as a NAND string. In recent years, NAND flash memory has been scaled in order to reduce cost per bit. However, as process geometries shrink, many design and process challenges are presented. These challenges include increased variability in transistor characteristics over process, voltage, and temperature variations.

BRIEF DESCRIPTION OF THE DRAWINGS

[0005] FIG. 1 depicts one embodiment of a NAND string.

[0006] FIG. 2 depicts one embodiment of the NAND string of FIG. 1 using a corresponding circuit diagram.

[0007] FIG. 3A depicts one embodiment of a memory block including a plurality of NAND strings.

[0008] FIG. 3B depicts one embodiment of possible threshold voltage distributions for a three-bit-per-cell memory cell.

[0009] FIG. 4A depicts one embodiment of a vertical NAND structure.

[0010] FIG. 4B depicts one embodiment of a cross-sectional view taken along line X-X of FIG. 4A.

[0011] FIG. 5A depicts one embodiment of a non-volatile storage system.

[0012] FIG. 5B depicts one embodiment of a sense block.

[0013] FIG. 6A depicts one embodiment of a portion of a sense amplifier for biasing a bit line to a particular bit line voltage.

[0014] FIG. 6B depicts one embodiment of a table showing various settings for a gate of an NMOS transistor in a source follower configuration.

[0015] FIG. 6C depicts one embodiment of a portion of a sense amplifier that may be used for biasing a bit line to a particular bit line voltage during a program verify operation.

[0016] FIG. 7A is a flowchart describing one embodiment of a process for performing a program verify operation.

[0017] FIG. 7B is a flowchart describing another embodiment of a process for performing a program verify operation.

DETAILED DESCRIPTION

[0018] Technology is described for verifying two or more programming states at the same time. In some cases, during a program verify operation, two or more memory cell programming states or memory cell threshold voltage levels may be concurrently verified by applying a word line voltage to a plurality of memory cells, applying two or more different bit line voltages to the plurality of memory cells, and sensing the plurality of memory cells while the two or more different bit line voltages are applied to the plurality of memory cells. The bit line voltages applied during the program verify operation may allow a first set of the plurality of memory cells to be sensed at a first verify voltage level and a second set of the plurality of memory cells to be sensed at a second verify voltage level different from the first verify voltage level while biasing the plurality of memory cells to the same word line voltage or control gate (CG) voltage. In one example, during the program verify operation, a first memory cell of the plurality of memory cells may be sensed to verify that the first memory cell has reached a first programming state (e.g., the B state) while a second memory cell of the plurality of memory cells is sensed to verify that the second memory cell has reached a second programming state different from the first programming state (e.g., the D state). Verifying two or more memory cell threshold voltage levels at the same time may reduce the number of program verify cycles required for verifying the programming states of the plurality of memory cells.

[0019] In one embodiment, each memory cell of a plurality of memory cells connected to a word line may be programmed to one of eight different programming states during one or more programming operations. Between programming operations or subsequent to the one or more programming operations, one or more program verify operations may be performed to verify the intermediary or final programming states for the plurality of memory cells. During a program verify operation of the one or more program verify operations, two or more memory cell threshold voltage levels may be concurrently verified. In one embodiment, a first verify level (e.g., 1V) may be applied to a first set of the plurality of memory cells while a second verify level greater than the first verify level (e.g., 2V) is applied to a second set of the plurality of memory cells. Verifying two different verify levels at the same time may allow the time required to verify programming states to be cut in half. In another embodiment, each memory cell of the plurality of memory cells may have one of eight different verify levels